REMARKS

The application has been reviewed in light of the Office Action dated August 3, 2005. Claims 1-11 were pending, with claim 1 being the sole claim in independent form. Claims 12-22 were previously canceled, without prejudice or disclaimer. By this Amendment, new claim 23 has been added, and claim 1 has been amended to clarify the claimed invention.

Claims 1, 2, 5-7, 10 and 11 were rejected under 35 U.S.C. §103(a) as allegedly unpatentable over U.S. Patent No. 4,783,738 to Li et al., in view of Patterson et al., "Computer Architecture - A Quantitative Approach", (2nd Edition 1996). Claims 1-11 were rejected under 35 U.S.C. §103(a) as allegedly unpatentable over U.S. Patent No. 5,430,885 to Kaneko et al., in view of Patterson. Claims 3, 4, 8 and 9 were rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Li in view of Patterson and in view of Kaneko.

Applicant has carefully considered the Examiner's comments and the cited art, and respectfully submits that independent claim 1 as amended is patentable over the cited art, for at least the following reasons.

This application relates to a parallel processor and/or image processing apparatus adapted for nonlinear processing. The application describes a feature which allows assorted SIMD (single instruction stream multiple data stream) instructions as well as non-linear processing to be performed efficiently.

For example, claim 1 of the present application is directed to a parallel processor comprising a global processor and a processor-element block comprising a plurality of processor elements. The global processor interprets a program and controls the entirety of the parallel processor. Each processor element comprises a register file and an operation array for processing a plurality of sets of data. The global processor assigns to the processor elements respective

processor-element numbers, and can output a control signal to the processor elements to set the assigned processor-element numbers corresponding to the processor elements as input values of the operation arrays, respectively. In addition, in the parallel processor of claim 1, the register file of a processor element holds plural sets of data for operation processing by the operation array of the processor element, and the operation array of a processor element includes a multiplexer coupled to the register file of the processor element and to the register files of respective adjacent processor elements. Thus, the global processor can instruct selected processor elements to perform non-linear processing on data retrieved from the register file of the selected processor element or from the register file of an adjacent processor element, according to processor element instructions from the global processor, while reducing the number of instruction execution cycles.

Li, as understood by Applicant, is directed to an array processor including an instruction adapter for the processing elements of the array processor. Each processing element has an arithmetic logic unit (ALU) and a local memory.

The Office Action acknowledged that Li does not disclose or suggest that the processing element of Li includes a register file of a processor element which holds plural sets of data for operation processing by the operation array of the processor element.

Kaneko, as understood by Applicant, is directed to a multi-processor system for multi-dimensional image signal processing. The system includes a host processor and plural co-processors. Each co-processor includes an arithmetic logic unit (ALU) and a local memory.

The Office Action acknowledged that Kaneko does not disclose or suggest that the co-processor of Kaneko includes a register file which holds plural sets of data for operation processing by the operation array of the processor element.

Patterson is cited in the Office Action as purportedly disclosing using a register file as a local memory to hold and supply data operands to a processor.

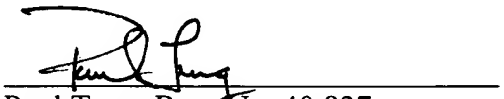
Applicant does not find teaching or suggestion in Li or Kaneko or Patterson, however, that the operation array of a processor element includes a multiplexer coupled to the register file of the processor element and to the register files of respective adjacent processor elements, as provided by amended claim 1.

In view of the amendments to the claims and remarks hereinabove, Applicant submits that the application is now in condition for allowance. Accordingly, Applicant earnestly solicits the allowance of the application.

If a petition for an extension of time is required to make this response timely, this paper should be considered to be such a petition. The Office is hereby authorized to charge any fees that may be required in connection with this amendment and to credit any overpayment to our Deposit Account No. 03-3125.

If a telephone interview could advance the prosecution of this application, the Examiner is respectfully requested to call the undersigned attorney.

Respectfully submitted,



Paul Teng, Reg. No. 40,837
Attorney for Applicant
Cooper & Dunham LLP
Tel.: (212) 278-0400